UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/044,185	01/09/2002	David B. Kramer	KRAMER 2-1-3	9779

47394 7590 08/03/2007

HITT GAINES, PC
ALCATEL-LUCENT
PO BOX 832570
RICHARDSON, TX 75083

EXAMINER	
MATTIS, JASON E	
ART UNIT	PAPER NUMBER
2616	

NOTIFICATION DATE	DELIVERY MODE
08/03/2007	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

docket@hittgaines.com

Office Action Summary	Application No.	Applicant(s)	
	10/044,185	KRAMER ET AL.	
	Examiner	Art Unit	
	Jason E. Mattis	2616	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 May 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action is in response to the amendment filed 5/21/07. Claims 1-20 are currently pending in the application.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-4, 6-11, 13-18, and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dell et al. (U.S. Publication US 2002/0085578 A1) in view of Krishna et al. (U.S. Publication US 2001/0050916 A1).

With respect to claims 1 and 8, Dell et al. discloses a non-blocking crossbar switch and method of operating a non-blocking crossbar switch **(See the abstract of Dell et al. for reference to crossbar devices and the method of operating the crossbar devices)**. Dell et al. also discloses inputs and outputs with each output having a destination FIFO buffer and a number of crossbar FIFO buffers corresponding to inputs **(See page 3 paragraphs 48-49, page 8 paragraph 107, and Figures 2 and 10 of Dell et al. for reference to crossbar device 206 having inputs connecting to**

ingress line cards 202 and outputs connecting to egress line cards 210 and for reference to each of the outputs ports having a corresponding FIFO queue, which is a FIFO buffer, and for reference to also having a number of routing FIFO queues, which are crossbar FIFO buffers, corresponding to inputs). Dell et al. further discloses a scheduler configured to cause a packets to be transmitted from one of the inputs toward one of the outputs only when both the destination FIFO buffer associated therewith and an interposing one of the crossbar FIFO buffers have sufficient memory to contain an a specific packet **(See pages 8-9 paragraphs 111-120, pages 9-10 paragraphs 128-137, and Figures 12 and 15-16 of Dell et al. for reference to input devices receiving grants to transmit cells, which are packets of a particular length, only when there is no back-pressure in corresponding FIFO queues meaning that a cell is transmitted toward the output only when all queues have enough memory to contain the packet)**. Dell et al. also discloses that the packets are unsegmented and of differing lengths **(See page 6 paragraphs 90-92 of Dell et al. for reference to encapsulating packets of variable size into switching cells to be transmitted through the switch fabric, and for reference to choosing a switching cell size such that packets do not need to be segmented into multiple cells)**. Although Dell et al. does disclose that the number of inputs, outputs, and queues associated with the inputs and outputs is programmable and changeable depending on system requirements **(See pages 6-8 paragraphs 93-104 of Dell et al. for reference to this programmability)**, Dell et al. does not specifically disclose that there are n inputs and n outputs with each output having n crossbar FIFO buffers.

With respect to claim 15, Dell et al. discloses a multi-channel network line card for packet-based networks **(See pages 3-4 paragraphs 47-53 and Figures 2-3 of Dell et al. for reference to line cards 202)**. Dell et al. also discloses at least three physical interfaces **(See pages 3-4 paragraphs 47-53 and Figures 2-3 of Dell et al. for reference to line cards 302 having at least 2 physical interfaces)**. Dell et al. further discloses network processors that convert a packet between protocols with the network processors coupled to corresponding ones of the interfaces **(See page 6 paragraphs 91-92 of Dell et al. for reference to the system having protocol independence by using network processors on the line cards to convert packets into a common protocol for use in the system)**. Dell et al. also discloses a non-blocking crossbar coupled to the network processors and physical interfaces **(See pages 3-4 paragraphs 47-53 and Figures 2-3 of Dell et al. for reference to a crossbar 206 being coupled to the line cards)**. Dell et al. also discloses inputs and outputs with each output having a destination FIFO buffer and a number of crossbar FIFO buffers corresponding to inputs **(See page 3 paragraphs 48-49, page 8 paragraph 107, and Figures 2 and 10 of Dell et al. for reference to crossbar device 206 having inputs connecting to ingress line cards 202 and outputs connecting to egress line cards 210 and for reference to each of the outputs ports having a corresponding FIFO queue, which is a FIFO buffer, and for reference to also having a number of routing FIFO queues, which are crossbar FIFO buffers, corresponding to inputs)**. Dell et al. further discloses a scheduler configured to cause a packet to be transmitted from one of the inputs toward one of the outputs only when both the destination FIFO buffer

associated therewith and an interposing one of the crossbar FIFO buffers have sufficient memory to contain and entirety of the packet **(See pages 8-9 paragraphs 111-120, pages 9-10 paragraphs 128-137, and Figures 12 and 15-16 of Dell et al. for reference to input devices receiving grants to transmit cells, which are packets of a particular length, only when there is no back-pressure in corresponding FIFO queues meaning that a cell is transmitted toward the output , only when all queues have enough memory to contain the packet)**. Dell et al. also discloses that the packets are unsegmented and of differing lengths **(See page 6 paragraphs 90-92 of Dell et al. for reference to encapsulating packets of variable size into switching cells to be transmitted through the switch fabric, and for reference to choosing a switching cell size such that packets do not need to be segmented into multiple cells)**. Although Dell et al. does disclose that the number of inputs, outputs, and queues associated with the inputs and outputs is programmable and changeable depending on system requirements **(See pages 6-8 paragraphs 93-104 of Dell et al. for reference to this programmability)**, Dell et al. does not specifically disclose that there are n inputs and n outputs with each output having n crossbar FIFO buffers.

With respect to claims 1, 8, and 15, Krishna et al., in the field of communications, discloses a crossbar having n inputs and n outputs with each output having n crossbar FIFO buffers **(See page 4 paragraph 53 and Figure 1 of Krishna et al. for reference to a crossbar having an equal number of inputs and outputs with each output having a corresponding output queue, or destination FIFO buffer,**

and n corresponding virtual output queues, or crossbar FIFO buffers). A crossbar having n inputs and n outputs with each output having n crossbar FIFO buffers has the advantage of allowing a destination FIFO buffer separate access to packets from each input such that packets may be sent to their destination in the most efficient manner order.

It would have been obvious for one of ordinary skill in the art at the time of the invention, when presented with the work of Krishna et al., to combine a crossbar having n inputs and n outputs with each output having n crossbar FIFO buffers, as suggested by Krishna et al., with the system and method of Dell et al., with the motivation being to allow a destination FIFO buffer separate access to packets from each input such that packets may be sent to their destination in the most efficient manner order.

With respect to claims 2-3, 9-10, and 17, Dell et al. discloses that the inputs and outputs are selected based on priority thereof **(See page 10 paragraphs 145-153 for reference to selecting both inputs and outputs based on priorities of the inputs and outputs)**.

With respect to claims 4, 11, and 18, Dell et al. discloses that the inputs are coupled to different types of packet based fabrics **(See page 2 paragraphs 11-12 and page 6 paragraphs 91-92 of Del et al. for reference to the system being protocol independent, meaning it supports connections to various packet based fabrics such as IP, ATM, and MPLS)**.

With respect to claims 6-7, 13-14, and 20, Dell et al. discloses an arbiter to select one of the crossbar FIFO buffers based upon packet priority and transfer a

packet to the destination FIFO buffer **(See page 8 paragraph 107 and page 10 paragraphs 145-153 of Dell et al. for reference to a arbiter selecting which bid to accept for transfer of a packet to an output FIFO queue and for reference to selecting a based on packet priority)**.

With respect to claim 16, Dell et al. discloses a fast pattern processor that receives, analyzes, and classifies the packet **(See page 8 paragraph 106 and page 12 paragraph 174 of Dell et al. for reference to a line card receiving packets, analyzing the packets, and classifying the packets based on type, priority, etc.)**. Dell et al. also discloses a routing switch processor that processes the packet, performs traffic management, and converts the packet into an appropriate protocol **(See page 6 paragraphs 91-92 of Dell et al. for reference to the network processor processing the packet by performing traffic management and by converting the packet into an appropriate protocol)**.

4. Claims 5, 12, and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dell et al. in view of Krishna et al. as applied to claims 1-4, 6-11, 13-18, and 20 above, and further in view of Chen et al. (U.S. Pat. 6975638 B1).

With respect to claims 5, 12, and 19, although Dell et al. does disclose connecting inputs and outputs to various types of networks **(See page 2 paragraphs 11-12 and page 6 paragraphs 91-92 of Del et al. for reference to the system being protocol independent, meaning it supports connections to various packet based fabrics such as IP, ATM, and MPLS)**, the combination of Dell et al. and Krishna et al.

does not disclose connecting the inputs and outputs to a SONET network and two Ethernet networks.

With respect to claims 5, 12, and 19, Chen et al. discloses a crossbar switch with inputs connected to Gigabit Ethernet networks and a SONET network **(See column 5 lines 7-18 and Figure 3 of Chen et al. for reference to a crossbar switching having inputs connected to Gigabit Ethernet networks and a SONET network)**. A crossbar switch with inputs connected to Gigabit Ethernet networks and a SONET network has the advantage of allowing the switch to transfer packet from both SONET and Ethernet network, which are highly used packet protocol networks.

It would have been obvious for one of ordinary skill in the art at the time of the invention, when presented with the work of Chen et al., to combine a crossbar switch with inputs connected to Gigabit Ethernet networks and a SONET network, as suggested by Chen et al., with the system and method of Dell et al. and Krishna et al., with the motivation being to allow the switch to transfer packet from both SONET and Ethernet network, which are highly used packet protocol networks.

Response to Arguments

5. Applicant's arguments filed 5/21/07 have been fully considered but they are not persuasive.

Regarding Applicant's argument that Dell does not disclose switching packets that are unsegmented and of differing lengths, the Examiner respectfully disagrees. As

shown in the rejections above, Dell et al. discloses transmitting variable sized packet through a switching fabric by encapsulating the packets into a fixed sized switching cell (See page 6 paragraphs 90-92 of Dell et al.). Dell et al. also discloses selecting the size of the fixed size switching cells such that packets do not have to be segmented into multiple switching cells (See page 6 paragraphs 90-92 of Dell et al.). Therefore, Dell et al. does disclose switching packets that are unsegmented and of differing lengths as claimed.

Regarding Applicant's argument that there is no motivation to combine the teachings of Dell et al. and Krishna et al., the Examiner respectfully disagrees. It is noted that it is only Krishna's teaching of a crossbar having n inputs and n outputs with each output having n crossbar FIFO buffers that is combined with the teachings of Dell et al. Since Dell et al. teaches the claimed scheduler transmitting unsegmented packets that are of differing lengths, this teaching does not need to be found in Krishna et al. Thus, there is motivation to combine the teachings of Dell et al. and Krishna et al. and the combined teachings do disclose all the claim limitations of the current independent claims, as shown in the rejections above.

Conclusion

6. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP

§ 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jason E. Mattis whose telephone number is (571) 272-3154. The examiner can normally be reached on M-F 8AM-5:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Huy Vu can be reached on (571) 272-3155. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

jem

HUY D. VU
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600